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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,204	07/18/2003	Warren E. Cory	X-1308 US	4026

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EXAMINER	
TRAN, KHANH C	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/622,204	CORY, WARREN E.	
	Examiner	Art Unit	
	Khanh Tran	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6-8,10,12-16,19-23 and 32* is/are rejected.

7)☒ Claim(s) *2, 5, 9, 11, 17-18 and 24-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 3-4, 6-8, 10, 12-16, 19-22 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Collins U.S. Patent 6,907,552 B2.

Regarding claim 1, in column 3 lines 25-55, Collins teaches a method and apparatus for relative dynamic skew compensation of parallel data lines. One embodiment of Collins teachings provides a system that performs a two-step skew compensation procedure as a training sequence by first correcting for any phase error alignment between the parallel link clock and data signal edges of each data channel, thereby allowing the received data bits to be correctly sampled. Then, a second step is performed to "word-align" the bits into the original format, which is accomplished with an SSM (Skew Synchronizing Marker) byte in a data FIFO of each data channel. The SSM byte is transmitted on each data channel and terminates the training sequence. When the SSM byte is detected by logic in the data FIFO of each data channel, the data FIFO employs the SSM byte to initialize the read and write pointers to properly align the output data.

Collins does not teach a master alignment marker and a slave alignment marker as claimed in the application claim.

As recited above, Collins teaches using a training sequence for correcting any phase error alignment between the parallel link clock and data signal edges of each data channel. Because each data channel is phase aligned with the parallel link clock, one of ordinary skill in the art at the time the invention was made would have recognized that any data channel can be designated as a master data channel and the rest of the data channels are slave data channel. Each SSM byte associating with a data channel corresponds to the claimed master alignment marker and slave alignment marker.

Collins does not explicitly teach the step of developing a model of skew in a slave channel based on the master alignment marker and slave alignment marker as claimed in the application claim.

As recited above, Collins teaches the step of performing "word-align" the bits into the original format, which is accomplished with an SSM (Skew Synchronizing Marker) byte in a data FIFO of each data channel using a training sequence. In view of the foregoing teachings, because of employing a training sequence, one of ordinary skill in the art at the time the invention was made would have recognized that the act of using a training sequence to perform word alignment would correspond to the step of developing a model of skew as set forth in the application claim.

In column 3 lines 40-50, Collins further teaches when the SSM byte is detected by logic in the data FIFO of each data channel, the data FIFO employs the SSM byte to

initialize the read and write pointers to properly align the output data. The foregoing teachings correspond aligning a slave channel at a time determined by the slave channel.

Regarding claims 3-4, due to skew in a parallel link at higher bandwidths, the SSM byte of a data channel can lead or lag the SSM byte of another data channel as appreciated by one of ordinary skill in the art.

Regarding claims 6-7, as recited in claim 1 rejection, in column 3 lines 40-50, Collins further teaches when the SSM byte is detected by logic in the data FIFO of each data channel, the data FIFO employs the SSM byte to initialize the read and write pointers to properly align the output data.

Regarding claim 8, in column 3 lines 45-65, Collins teaches at the link source node, an SSD (Source Synchronous Driver) formats "M" bits of input data received from the core logic and drives "M" data channels onto the physical link along with a link clock. The "M" data bits and link clock are received at the link destination node by a Dynamic Skew Compensation (DSC) architectural block that compensates for skew, re-centers the link clock edge relative to the bits of data, and outputs "M" bits of data. In order to compensate for skew, the read clock has to move a number of bytes equal to the skew as appreciated by one of ordinary skill in the art.

Regarding claim 10, because the data FIFO employs the SSM byte to initialize the read and write pointers to properly align the output data. The skew model is not affected by the adjustment to the pointer.

Regarding claim 12, in column 9 lines 10-30, as shown in FIG. 3, a transmitter 300 comprises one or more Source Synchronous Driver (SSD) Modules 310-0, 310-1, ... 310-N, each of which divides data into a plurality of bytes to be transmitted in separate communication channels 0 1 2 3.

Regarding claim 13, claim is rejected on the same ground as for claim 1 in view of claim 8 because of similar scope.

Regarding claim 14, as recited in claim 1 rejection, the two-step skew compensation procedure first corrects for any phase error alignment between *the parallel link clock and data signal edges* of each data channel, thereby allowing the received data bits to be correctly sampled. Then, a second step is performed to "word-align" the bits into the original format, which is accomplished with an SSM (Skew Synchronizing Marker) byte in a data FIFO of each data channel. In light of the foregoing teachings, one of ordinary skill in the art at the time the invention was made would have recognized that the word alignment would involve in counting a number of clock cycles in reference to the parallel link clock.

Regarding claims 15-16, claims are rejected on the same ground as for claims 3-4 because of similar scope.

Regarding claim 19, as recited in claim 1 rejection, Collins teaches a two-step skew compensation procedure by first correcting for any phase error alignment between the parallel link clock and data signal edges of each data channel, thereby allowing the received data bits to be correctly sampled. Then, a second step is performed to "word-align" the bits into the original format, which is accomplished with an SSM (Skew Synchronizing Marker) byte in a data FIFO of each data channel. In light of the foregoing teaching, the minimum period is the time for performing the phase error alignment.

Regarding claim 20, claim is rejected on the same ground as for claim 1 in view of claim 8 because of similar scope. Furthermore, in column 9 line 60 via column 10 line 5, Collins teaches depending on the DSC-to-core interface desired, *control logic* of the DSC Data Channels 610-0, 610-1, 610-2, 610-3, . . . receives part or all of the broadcast status signals and controls the rd_cnt_enb signal to the Read Pointer 1110 shown in FIG. 11 to advance or hold the Read-Pointer address; see also FIG. 6.

Regarding claim 21, as recited in claim 1 rejection, Collins further teaches when the SSM byte is detected by logic in the data FIFO of each data channel, the data FIFO employs the SSM byte to initialize the read and write pointers to properly align the

output data. The foregoing teachings correspond aligning a slave channel at a time determined by the slave channel.

Regarding claim 22, FIG. 8 discloses the Dynamic Skew Compensation (DSC) block includes a finite state machine (FSM) 860.

Regarding claim 32, FIG. 3 discloses a plurality of data channels 0, 1, ..., M, each having a FIFO and a Dynamic Skew Compensation block; see column 3 lines 50-60 and column 9 lines 1-45.

2. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Collins U.S. Patent 6,907,552 B2 as applied to claim 22 and further in view of Harry Newton, Newton's Telecom Dictionary, ISBN Number 1-57820-069-5, Seventeenth Edition, February 2001.

Regarding claim 23, Collins does not explicitly teach the Dynamic Skew Compensation (DSC) block comprsing a microprocessor.

According to Newton's Telecom Dictionary on page 281, a Finite State Machine is a computer with a defined set of possible states and defined transitions from state to state. In view of that, one of ordinary skill in the art at the time the invention was made would have recognized that the Dynamic Skew Compensation (DSC) block includes a microprocessor.

Allowable Subject Matter

3. Claims 2, 5, 9, 11, 17-18 and 24-31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Li et al. U.S. Patent 6,944,691 B1 discloses "Architecture That Converts A Half-Duplex Bus To A Full-Duplex Bus While Keeping The Bandwidth Of The Bus Constant".

Lerner U.S. Patent 7,103,071 B1 discloses "Communication Protocol For The Broadcast Of First/Last Event Detection Over A Single Communication Channel".

Robinson et al. U.S. Patent 5,856,999 discloses "Apparatus And Method For Data Transmission On Bonded Data Channels Of A Communications Network Utilizing A Single Serial Communications Controller".

Perumal et al. U.S. Patent 7,106,760 B1 discloses "Channel Bonding In SHDSL Systems".

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KCT

Khanh cong Tran 01/02/2007

Khanh Tran
Primary Examiner